

# AI-Based Signal Analyzer & Equalizer

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## Background

- **The High-Speed Challenge:** As data rates exceed **1GSPS**, signals suffer from severe degradation due to **impedance mismatches** and parasitic effects.
- **The Cost Barrier:** Traditional validation requires expensive instrumentation (VNAs, High-End Oscilloscopes) that cost \$100k+.
- **The Efficiency Gap:** Manual troubleshooting is time-consuming and requires expert analysis to identify the root cause of signal failure.

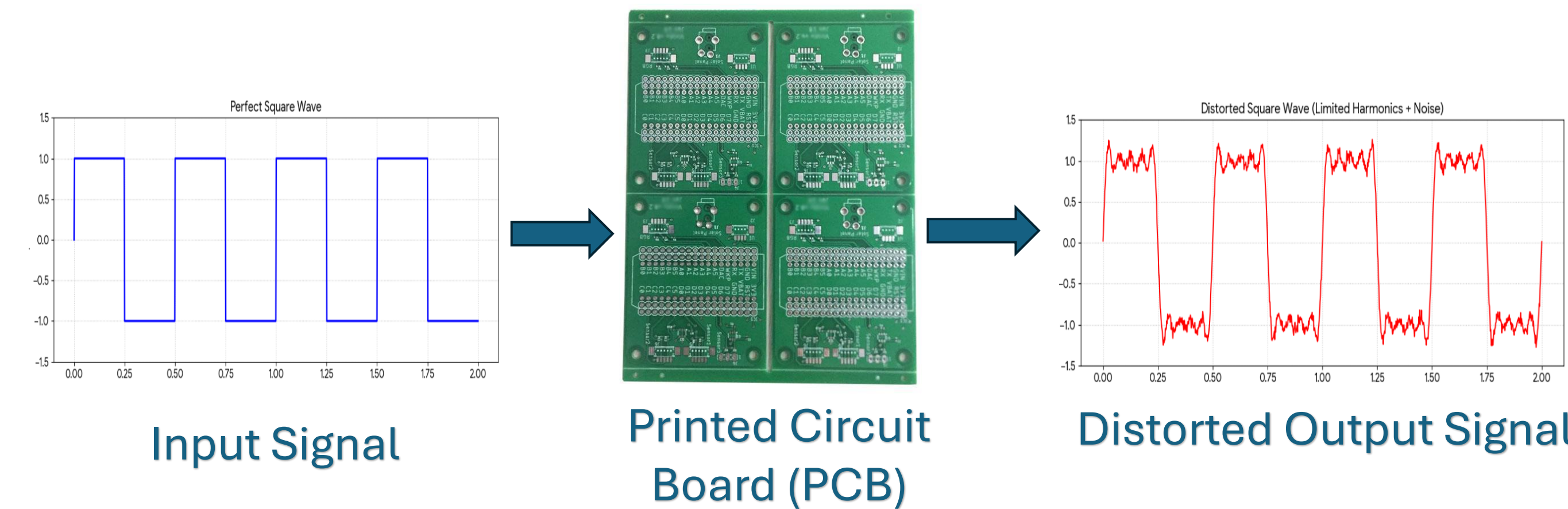


Figure 1: Signal degradation through a physical PCB channel

## Objectives

**The Goal:** Develop a single AI model that simultaneously analyzes signal health metrics and reconstructs distorted PCB signals in real-time

### Design Constraints

- Data Rate: 2.5 GSPS
- ADC Sampling: 12.5 GSPS
- System BW: 6.5 GHz minimum

### Measures of Success

- Analysis Accuracy:  $\leq 5$  MAE (Impedance, Eye Width/Height, Jitter, SNR)
- Reconstruction:  $\leq 5\%$  NMSE

## Proposed Solution

**Shared Backbone:** A single PyTorch neural network extracts features from raw data.

**Parallel Outputs:** Calculates Impedance, Jitter, SNR, and Eye margins simultaneously.

**FPGA Integration:** Hardware applies real-time signal equalization.

**Signal Recovery:** Converts a degraded "closed-eye" input into a clean "open-eye" output.

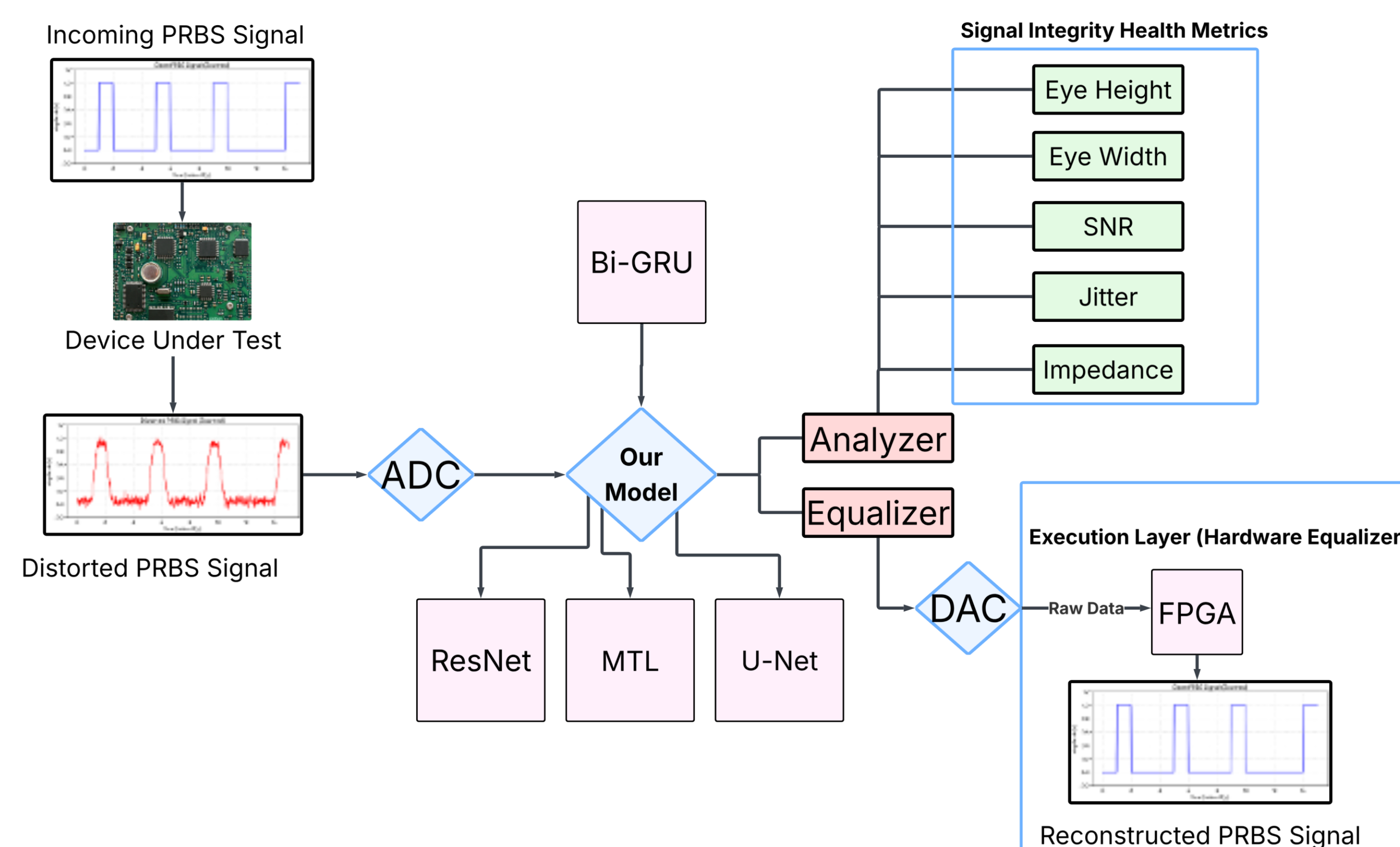


Figure 2: Proposed Solution Workflow

## Methodology

### 1. Automated Data Generation

- Used **Python/AEL** to automate the generation of thousands of **Keysight ADS** signal profiles.
- Dataset includes diverse board configurations: **Deterministic and random jitter**, various **trace widths, lengths, and spacings**.

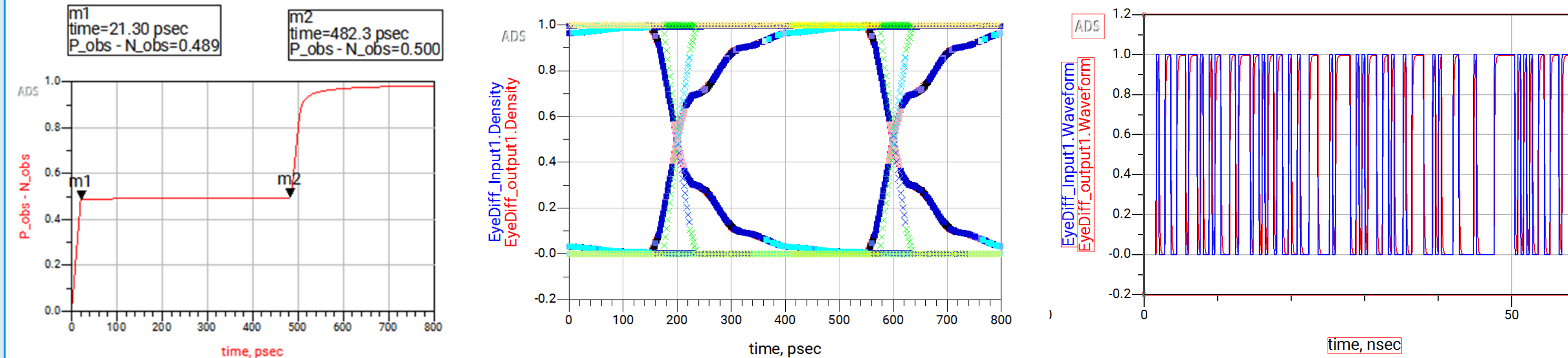


Figure 3: Automated data generation and metric extraction.(TDR, Eye and Channel plots)

### 2. AI Model & Training Pipeline

**Architecture:** Developed a **Multi-Task Learning (MTL)** model in **PyTorch**.

**Shared Backbone:** A four-block **ResNet encoder** extracts universal features from raw 32,768-sample bitstreams.

#### Task-Specific Heads:

- **Analyzer (Regression):** Predicts 5 SI health metrics: **Impedance, Jitter RMS, SNR, Eye Height, and Eye Width**.
- **Equalizer (Reconstruction):** Uses a **U-Net decoder** with skip connections to restore the distorted signal to its original "clean" state.

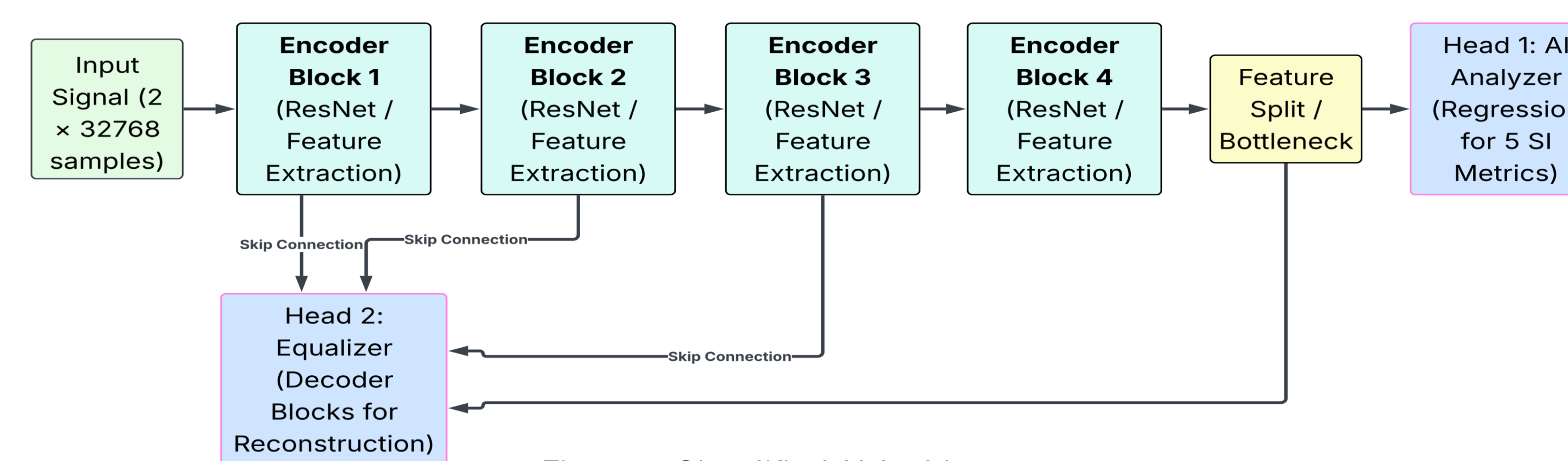


Figure 4: Simplified AI Architecture

### 3. Physical Validation & Setup

**Hardware:** Utilized a high-speed **Bit Error Rate Tester (BERT)** to generate PRBS signal and High bandwidth **Oscilloscope** for real-world validation.

**Signal Capture:** Measured **2.5 Gbps** signals at a **20 GSPS** sampling rate to ensure high-frequency detail.

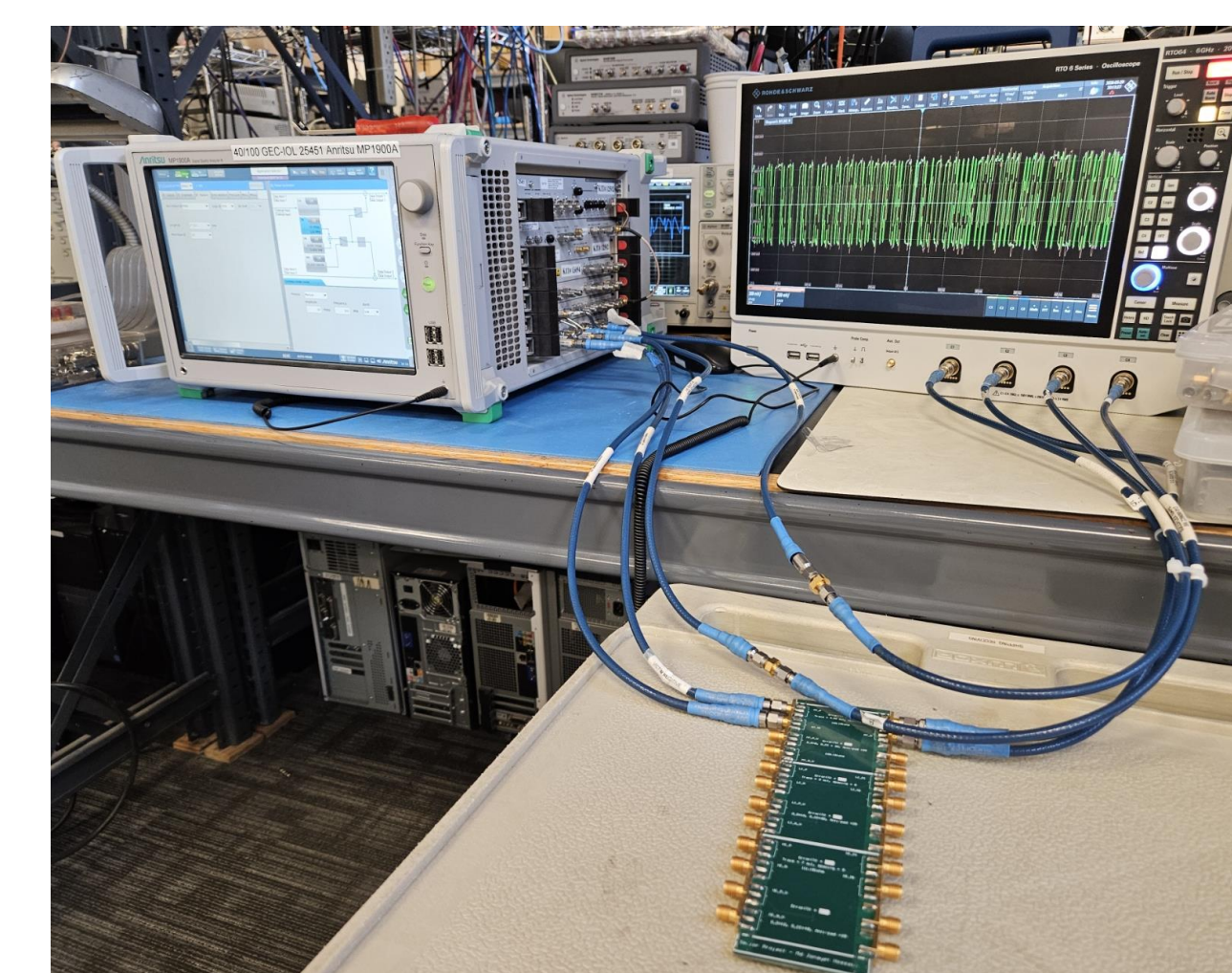


Figure 5: Physical Set-up with the Test board

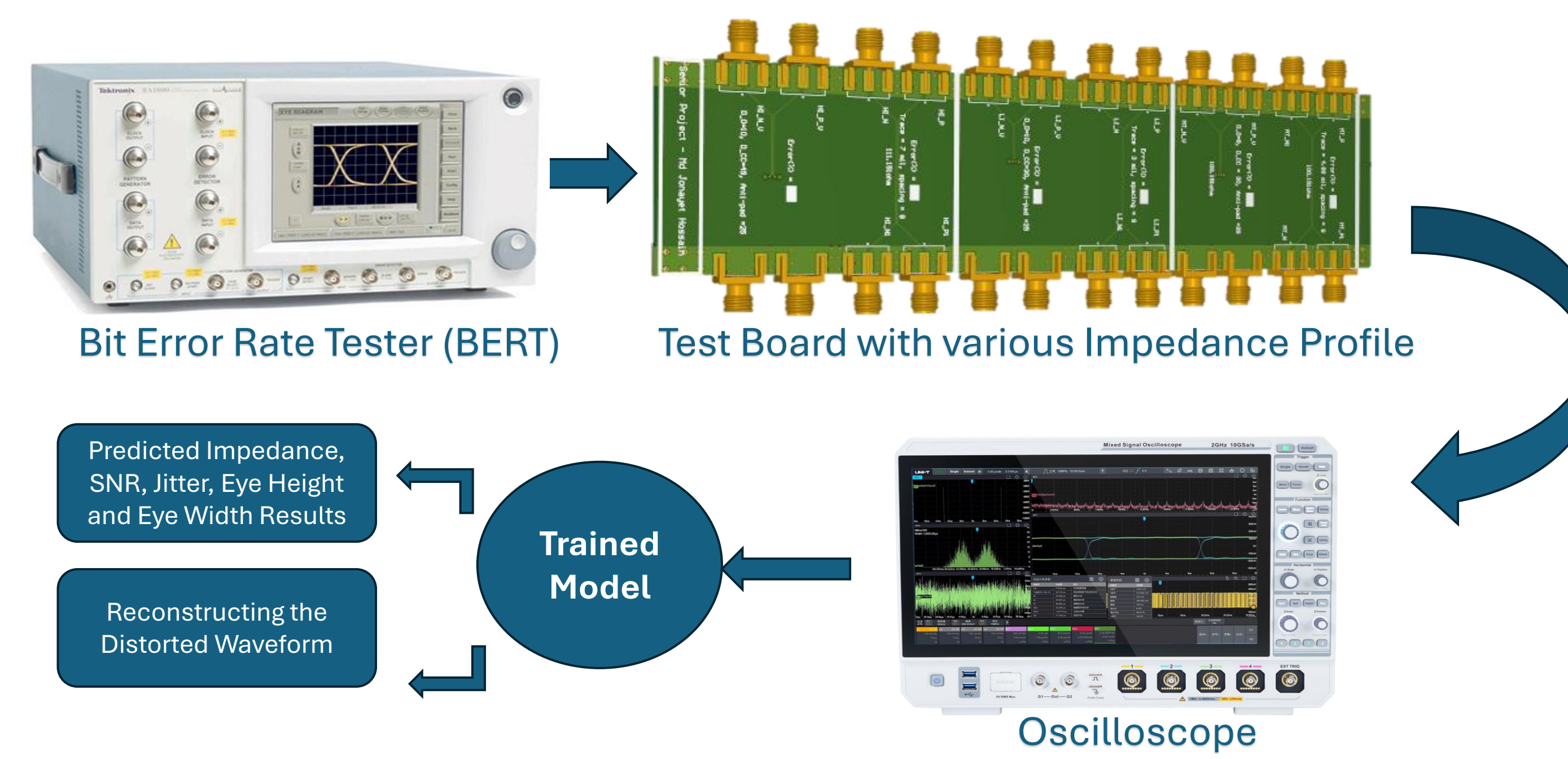


Figure 6: Physical hardware validation setup using a BERT, Oscilloscope and test fixture

## Results

### Equalizer Performance (Success):

- **High-fidelity recovery:** The AI successfully matched the clean input signal.
- **Distortion removed:** Effectively eliminated "ringing" and "rounding" from the distorted output, meeting the **5% NMSE** constraint.

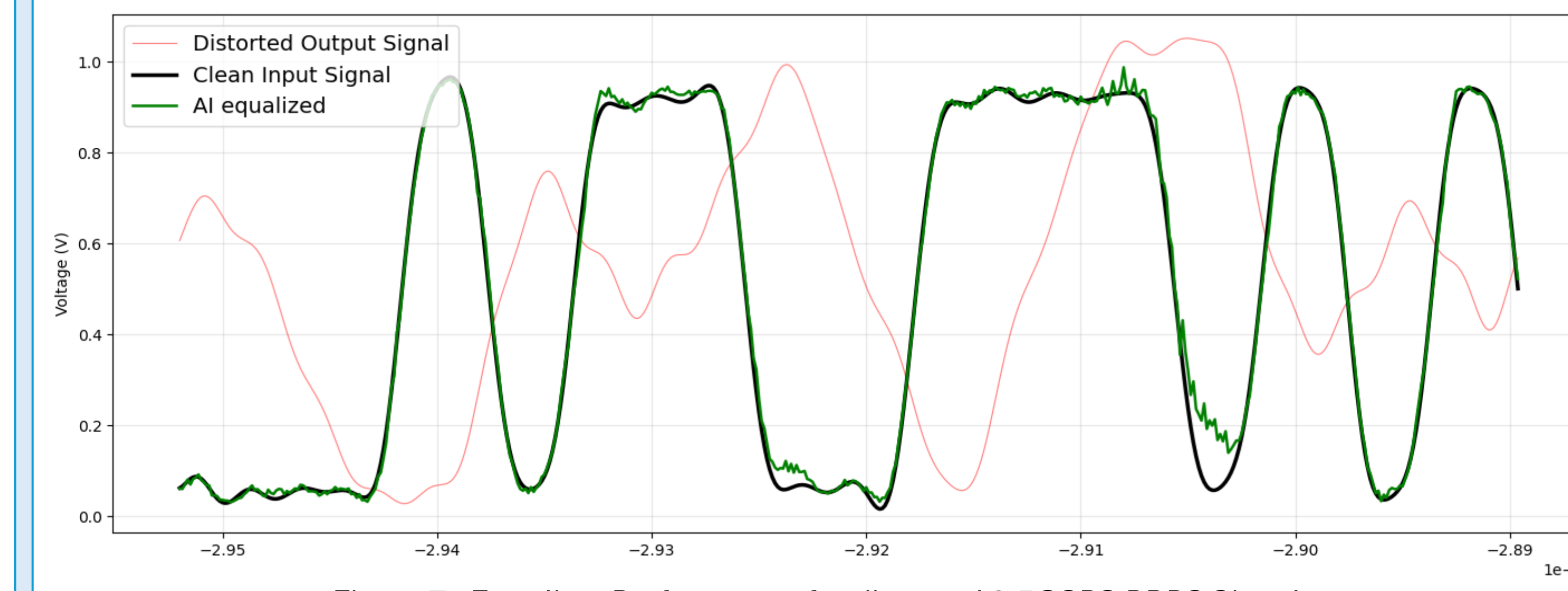


Figure 7: Equalizer Performance for distorted 2.5GSPS PRBS Signal

### Impedance Prediction (Mixed Results):

- **Constraint Not Met:** Failed to achieve the **5 MAE** accuracy.
- **Matched (Perfect) Impedance:** Showed notable error even under ideal conditions (e.g., 6.89  $\Omega$  error at 300 MSPS).
- **Mismatched Impedance:** Performance degraded further, with errors peaking at 16.8  $\Omega$  during high-speed (2.5 GSPS) operation.
- **Conclusion:** The analyzer requires significant retraining to meet the strict accuracy constraints for this system.

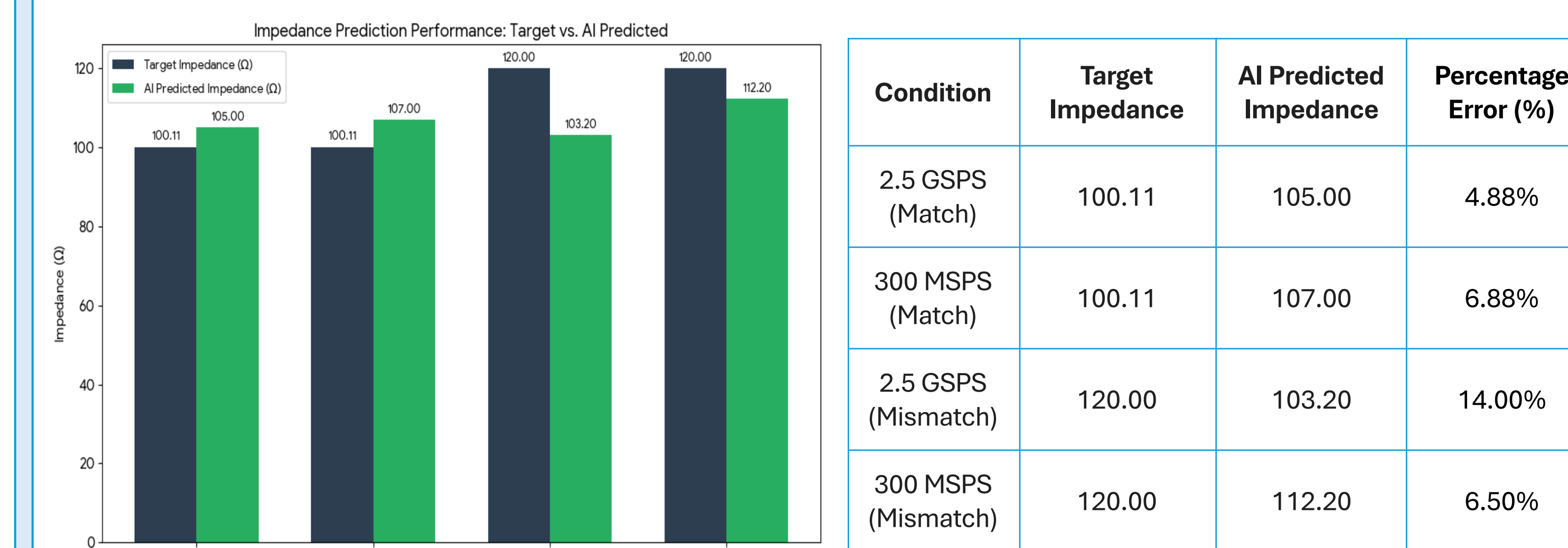


Figure 8: Analyzer Performance for Impedance evaluation (2.5GSPS & 300MSPS)

## Conclusion & Future Work

While the AI Equalizer successfully recovered distorted signals to meet the **5% NMSE** constraint, the Analyzer fell short of the **5 MAE** impedance prediction limit and requires further retraining. Moving forward, the optimized model will be **synthesized onto an FPGA** with high-speed ADCs and DACs to create a real-time, self-correcting system that actively maintains signal integrity in live hardware.

## References

- [1] Prerna, Nithya Ramalingam, Zaman Zaid Mulla, Archana Ganeshan, Ranjul Balakrishnan, and Anoop Karunan. "Artificial Intelligence-based advanced Signal Integrity prediction." 2022 6th International Conference on Devices, Circuits and Systems (ICDCS) (2022).
- [2] Keysight Technologies, "PathWave Advanced Design System (ADS)," 2025.
- [3] S. Srivallapanondh et al., "Multi-Task Learning to Enhance Generalizability of Neural Network Equalizers," *IEEE Photonics Technology Letters*, 2023.